REMARKS

This responds to the Office Action mailed on 19 October 2006 and the Advisory Action mailed 18 January 2007. It is noted that the Applicant's amendments made in the response to final Office Action filed 05 January 2007 were not entered.

Claim 1, 3, 5 and 7-11 are amended; no claims are canceled; and claims 17-20 are added. As a result, claims 1-20 are now pending in this application. No new matter has been added.

§102 Rejection of the Claims

Claim 1 was rejected under 35 U.S.C. § 102(b) for anticipation by Beard et al. (US 5,430,884, hereinafter "Beard").

Beard describes a method for fetching instructions in an high performance scalar/vector processor. Specifically, Beard describes "issuing" vector instructions from a scalar processor (102) to a vector processor (104) and "initiating" the vector instruction issued from the scalar processor in the vector processor (104) (Figs 2 & 3 and col. 3, lines 27-41).

Applicant respectfully submits that Beard does not teach following elements as taught by Applicant and claimed in claim 1: (1) dispatching a vector instruction from a scalar processing unit to a vector processing unit even if all scalar operands are not ready; and (2) predispatching, within the vector processing unit, the vector instruction received from the scalar processing unit if all previously received vector instructions are scalar committed. Claim 1 has been amended to more clearly define its claimed invention.

In the Office Action, the Examiner asserts that Beard teaches the two elements (dispatching from the scalar processing unit and predispatching in the vector processing unit) as described and claimed by Applicant (Office Action, p. 3, # 6, lines 6-15 and p. 24, # 26, lines 5-10). As support of this, the Examiner points to col. 3, lines 27-30 of Beard, which states:

> (lines 27-30) A vector instruction is decoded and **issued** and transferred [from the scalar processor unit] to a queue in the vector processor unit of the processor **when its scalar operand data, if any, is available** and the queue is not full...

Specifically, the Examiner argues that the issue process under Beard's approach discloses the dispatch from the scalar processing unit under Applicant's approach. In addition, the Examiner

argues that the predispatch in the vector dispatch unit under Applicant's approach is also shown by Beard's issue process because the predispatch occurs at the same time as the dispatch from the scalar processing unit under Applicant's approach. *See* also Advisory Action, p. 2, Continuation of 11, lines 7-9.

Applicant respectfully disagrees with the Examiner's interpretation of Beard and Applicant's claimed invention. First of all, as quoted above, the cited portion shows that Beard issues a vector instruction from the scalar processor to the vector processor when all required scalar data are available. In contrast, as noted at p. 15, line 28 through p. 16, line 24, Applicant teaches and claims dispatching a vector instruction from the scalar processing unit to the vector processing unit even if all required scalar operands are not ready.

Secondly, unlike the Examiner's assertion, the predispatch does not occur at the same time as the dispatch under Applicant's approach. For example, as noted at p. 15, line 28 through p. 16, line 2, Applicant teaches that the Dispatch Unit (DU) in the scalar processing unit dispatches vector instructions to the Vector Dispatch Unit (VDU) in the vector processing unit. Applicant further teaches that the vector instructions received from the DU are predispatched within the VDU after all previous vector instructions are scalar committed. *Id.* Under Applicant's approach, therefore, the predispatch is executed by the vector processing unit not by the scalar processing unit used for the dispatch. Furthermore, the predispatch occurs at a time different from that of the dispatch because all previous vector instructions are required to be scalar committed for a vector instruction received from the scalar processing unit to be predispatched. Applicant is unable to find such a teaching in Beard.

For the reasons discussed above, Beard does not teach a method for decoupling operations among the scalar, vector load/store and vector execution units as taught by Applicant and claimed in claim 1. Reconsideration is respectfully requested.

§103 Rejection of the Claims

Claims 2-4, 7 and 12-16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard in view of Patterson et al (hereinafter "Patterson").

Beard is discussed above.

Patterson describes use of a date cache and an instruction cache along with a register, address translation and dealing with a translation fault, and use of a vector load/store unit in a scalar/vector processing computer system.

As noted in the discussion of claim 1 above, claims 2-4, 7 and 12-16 are patentable since none of the cited references, alone or in combination, teach or suggest the following elements as taught by Applicant and claimed in claim 2-4, 7 and 12-16: (1) dispatching a vector instruction from a scalar processing unit to a vector processing unit even if all scalar operands are not ready; and (2) predispatching, within the vector processing unit, the vector instruction received from the scalar processing unit if all previously received vector instructions are scalar committed.

Claims 5, 6, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard in view of Gharachorloo et al (hereinafter "Gharachorloo").

Beard is discussed above.

Gharachorloo describes using a reservation station and reorder buffers for renaming registers.

As noted in the discussion of claim 1, claims 5, 6, 8 and 9 are patentable since neither Beard nor Charachorloo, alone or in combination, teach or suggest the following elements as taught by Applicant and claimed in claims 5, 8 and 9: (1) dispatching a vector instruction from a scalar processing unit to a vector processing unit even if all scalar operands are not ready; and (2) predispatching, within the vector processing unit, the vector instruction received from the scalar processing unit if all previously received vector instructions are scalar committed.

Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Beard and Gharachorloo, further in view of Patterson.

As noted in the discussion of claim 1, claims 10 and 11 are patentable since none of the cited references, alone or in combination, teach or suggest the following elements as taught by Applicant and claimed in claims 10 and 11: (1) dispatching a vector instruction from a scalar processing unit to a vector processing unit even if all scalar operands are not ready; and (2) predispatching, within the vector processing unit, the vector instruction received from the scalar processing unit if all previously received vector instructions are scalar committed.

Claims 17-20 are added in this amendment. The limitations in the new claims 17-20 are fully supported from Applicant's Specification (e.g., Spec. p. 13, lines 11-13 and p. 16, lines 6-7, 14-17 & 22-24).

The new claims 17-20 are patentable as being dependent on a patentable base claim. In addition, none of the cited references, alone or in combination, teach or suggest marking vector instructions complete at a different time depending on whether they are memory instructions and whether they require scalar operands as taught by Applicant and claimed in claims 17-20. Applicant is unable to find such a teaching in any of the cited references. Allowance of claims 17-20 is respectfully requested.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612) 373-6909 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Reservation of Rights

In the interest of clarity and brevity, Applicant may not have addressed every assertion made in the Office Action. Applicant's silence regarding any such assertion does not constitute any admission or acquiescence. Applicant reserves all rights not exercised in connection with

this response, such as the right to challenge or rebut any tacit or explicit characterization of any reference or of any of the present claims, the right to challenge or rebut any asserted factual or legal basis of any of the rejections, the right to swear behind any cited reference such as provided under 37 C.F.R. § 1.131 or otherwise, or the right to assert co-ownership of any cited reference. Applicant does not admit that any of the cited references or any other references of record are relevant to the present claims, or that they constitute prior art. To the extent that any rejection or assertion is based upon the Examiner's personal knowledge, rather than any objective evidence of record as manifested by a cited prior art reference, Applicant timely objects to such reliance on Official Notice, and reserves all rights to request that the Examiner provide a reference or affidavit in support of such assertion, as required by MPEP § 2144.03. Applicant reserves all rights to pursue any cancelled claims in a subsequent patent application claiming the benefit of priority of the present patent application, and to request rejoinder of any withdrawn claim, as required by MPEP § 821.04.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Commissioner of Patents, P.O. Box 1450, Alexandria, VA ~~22313-~~1450 on this 16 day of February 2007.

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